Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 21 as follows:

Listing of Claims:

1. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a memory controller coupled to the memory devices;

at least one receive interface coupled to the memory controller; and

at least one transmit interface coupled to the memory controller to transmit memory transactions from the memory module, each transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits, each transmit interface including a data organization system organizing the command header and data into lane groups each of which includes a plurality of lanes each of which contains a plurality of parallel command header bits or parallel data bits, the data organization system organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits, the data organization system being operable to convert each of the lane groups into a serial stream of the lanes for transmission by the transmit interface, each of the transmitted lanes containing a plurality of parallel command header bits or parallel data bits.

2. (Original) The memory module of claim 1 wherein each of the lane groups comprise eight lanes.

3. (Original) The memory module of claim 1 wherein each of the lanes comprise 32 parallel bits of command header or data.

4. (Original) The memory module of claim 1 wherein the at least one transmit interface comprises an upstream transmit interface and a downstream transmit interface each of which comprises the data organization system.

5. (Original) The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

6. (Original) The memory module of claim 1 wherein the data organization system comprises:

a data organization unit organizing the command header and data into lane groups each of which includes a plurality of lanes containing either a command header or data, the data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits; and

a parallel-to-serial converter converting each of the lane groups into a serial stream of the lanes for transmission by the transmit interface.

7. (Original) The memory module of claim 6 wherein the data organization unit comprises:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

8. (Original) The memory module of claim 7, wherein the data organization unit further comprises:

a multiplexer coupled to receive the data stored in the data buffer for each of the transactions and the command headers stored in the command queue for each of the transactions,

the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals;

an arbitration unit coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a lane group of either data or a command header and data for at least one of the transactions to the output port of the multiplexer.

9. (Original) The memory module of claim 8 further comprising a parallel-to-serial converter coupled to the output port of the multiplexer, the parallel-to-serial converter being operative to convert the lane group at the output port of the multiplexer into a serial stream of the lanes.

10. (Original) The memory module of claim 1 wherein the data organization unit is configurable to vary the number of lanes in each lane groups that are coupled from the data organization during each cycle of a clock signal.

11. (Original) The memory module of claim 1 wherein the command header and data for each of the transactions comprise a memory packet.

12. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a memory controller coupled to the memory devices;

at least one receive interface coupled to the memory controller; and

at least one transmit interface coupled to the memory controller to transmit memory transactions from the memory module, each transmit interface receiving memory transactions each of which comprises a command header and data having a

variable number of data bits, each transmit interface including a data organization system that is operable to organize the command header and data into groups each of which contains a predetermined number of sub-groups of a predetermined size, each of the sub-groups containing a plurality of parallel command header bits or data bits, each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits, the data organization system further being operable to output each group of data as a serial stream of the sub-groups.

13. (Original) The memory module of claim 12 wherein each of the groups comprise eight sub-groups.

14. (Original) The memory module of claim 12 wherein each of the sub-groups comprise 32 parallel bits of command header or data.

15. (Original) The memory module of claim 12 wherein the at least one transmit interface comprises an upstream transmit interface and a downstream transmit interface each of which comprises the data organization system.

16. (Original) The memory module of claim 12 wherein the memory devices comprise dynamic random access memory devices.

17. (Original) The memory module of claim 12 wherein the data organization system comprises:

a data organization unit organizing the command header and data into groups each of which includes a plurality of the sub-groups containing either a command header or data, the data organization unit organizing the groups so that all of the sub-groups in each group are filled with either command header bits or data bits; and

a parallel-to-serial converter converting each of the groups into a serial stream of the sub-groups for transmission by the transmit interface.

18. (Original) The memory module of claim 17 wherein the data organization unit comprises:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

19. (Original) The memory module of claim 18, wherein the data organization unit further comprises:

a multiplexer coupled to receive the data stored in the data buffer for each of the transactions and the command headers stored in the command queue for each of the transactions, the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals;

an arbitration unit coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a group of sub-groups containing either data or a command header and data for at least one of the transactions to the output port of the multiplexer.

20. (Original) The memory module of claim 19 further comprising a parallel-to-serial converter coupled to the output port of the multiplexer, the parallel-to-serial

converter being operative to convert the group at the output port of the multiplexer into a serial stream of the sub-groups.

21. (Currently Amended) The memory module of claim 17 wherein the data organization unit is configurable to vary the number of ~~lanes~~sub-groups in each ~~lane~~ groups that are coupled from the data organization during each cycle of a clock signal.

22. (Original) The memory module of claim 12 wherein the command header and data for each of the transactions comprise a memory packet.

23. (Original) A data organization system, comprising:

a data organization unit organizing a command header and data for each of a plurality of memory transaction into lane groups each of which includes a plurality of lanes each of which contains a plurality of parallel command header bits or parallel data bits, the data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits; and

a parallel-to-serial converter converting each of the lane groups into a serial stream of the lanes each of which contains a plurality of parallel command header bits or parallel data bits.

24. (Original) The data organization system of claim 23 wherein each of the lane groups comprise eight lanes.

25. (Original) The data organization system of claim 23 wherein each of the lanes comprise 32 parallel bits of command header or data.

26. (Original) The data organization system of claim 23, further comprising:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

27. (Original) The data organization system of claim 26, wherein the data organization unit further comprises:

a multiplexer coupled to receive the data stored in the data buffer for each of the transactions and the command headers stored in the command queue for each of the transactions, the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals;

an arbitration unit coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a lane group of either data or a command header and data for at least one of the transactions to the output port of the multiplexer.

28. (Original) The data organization system of claim 23 wherein the data organization unit is configurable to vary the number of lanes in each lane groups that are coupled from the data organization during each cycle of a clock signal.

29. (Original) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory hub controller coupled to the processor bus;

a plurality of memory modules coupled to the memory hub controller by at least one bus, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub, comprising:

a memory controller coupled to the memory devices;

a receive interface coupled to the memory controller through a bus system; and

a transmit interface coupled to the memory controller through the bus system to transmit memory transactions from the memory module to the memory controller, the transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits, the transmit interface including a data organization system organizing the command header and data into lane groups each of which includes a plurality of lanes each of which contains a plurality of parallel command header bits or parallel data bits, the data organization system organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits, the data organization system being operable to convert each of the lane groups into a serial stream of the lanes for transmission by the transmit interface, each of the transmitted lanes containing a plurality of parallel command header bits or parallel data bits.

30. (Original) The processor-based system of claim 29 wherein each of the lane groups comprise eight lanes.

31. (Original) The processor-based system of claim 29 wherein each of the lanes comprise 32 parallel bits of command header or data.

32. (Original) The processor-based system of claim 29 wherein the bus system comprises a downstream bus for coupling memory transactions transmitted by the memory modules away from the memory controller and an upstream bus for coupling memory transactions transmitted by the memory modules toward the memory controller, and wherein the transmit interface comprises an upstream transmit interface coupled to the upstream bus and a downstream transmit interface coupled to the downstream bus, each of the upstream and downstream transmit interfaces including a respective one of the data organization systems.

33. (Original) The processor-based system of claim 29 wherein the memory devices comprise dynamic random access memory devices.

34. (Original) The processor-based system of claim 29 wherein the data organization system comprises:

a data organization unit organizing the command header and data into lane groups each of which includes a plurality of lanes containing either a command header or data, the data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits; and

a parallel-to-serial converter converting each of the lane groups into a serial stream of the lanes for transmission by the transmit interface.

35. (Original) The processor-based system of claim 34 wherein the data organization unit comprises:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

36. (Original) The processor-based system of claim 35, wherein the data organization unit further comprises:

a multiplexer coupled to receive the data stored in the data buffer for each of the transactions and the command headers stored in the command queue for each of the transactions, the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals;

an arbitration unit coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a lane group of either data or a command header and data for at least one of the transactions to the output port of the multiplexer.

37. (Original) The processor-based system of claim 36 further comprising a parallel-to-serial converter coupled to the output port of the multiplexer, the parallel-to-serial converter being operative to convert the lane group at the output port of the multiplexer into a serial stream of the lanes.

38. (Original) The processor-based system of claim 34 wherein the data organization unit is configurable to vary the number of lanes in each lane groups that are coupled from the data organization during each cycle of a clock signal.

39. (Original) The processor-based system of claim 29 wherein the command header and data for each of the transactions comprise a memory packet.

40. (Original) A method of transmitting memory transactions each of which comprises a command header and a variable amount of data, the method comprising:

organizing the command header and data into groups each of which contains a predetermined number of sub-groups of a predetermined size, each of the sub-groups containing a plurality of parallel command header bits or data bits, each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits; and

transmitting each group of data as a serial stream of the sub-groups each of which includes the plurality of parallel command header bits or data bits.

41. (Original) The method of claim 40 wherein the act of organizing the command header and data into groups comprises organizing the command header and data into groups each of which contains eight sub-groups.

42. (Original) The method of claim 40 wherein the act of organizing the command header and data into groups containing a predetermined number of sub-groups comprises the command header and data so that each sub-group comprises 32 parallel bits of command header or data.

43. (Original) The method of claim 40, further comprising varying the quantity of sub-groups in each group.

44. (Original) A method of transmitting memory transactions each of which comprises a command header and a variable amount of data, the method comprising organizing the command header and data into lane groups each of which contains a plurality of

lanes of a predetermined size, each of the lanes containing a plurality of parallel command header bits or data bits, the lane groups being organizing so that all of the lanes in each lane group are filled with either command header bits or data bits.

45. (Original) The method of claim 44 further comprising converting each of the lane groups into a serial stream of the lanes each of which contains a plurality of parallel command header bits or parallel data bits.

46. (Original) The method of claim 44 wherein the act of organizing the command header and data into lane groups comprises organizing the command header and data into lane groups each of which contains eight lanes.

47. (Original) The method of claim 44 wherein the act of organizing the command header and data into lane groups each of which contains a predetermined number of lanes comprises organizing the command header and data so that each lane comprises 32 parallel bits of command header or data.

48. (Original) The method of claim 44, further comprising varying the number of lanes in each lane group.